# INVESTIGATION OF THE OPTOELECTRONIC PROPERTIES OF CRYSTALLINE SILICON TEXTURED BY MASKLESS PLASMA ETCHING AT DIFFERENT IGNITION MODES

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ABSTRACT: Plasma etch processes for dry, maskless micro-structuring of monocrystalline silicon at temperatures above 0 °C for effective light absorption as well as passivation properties are investigated with respect to photovoltaic applications. Focused on the ignition mode, silicon samples are etched by two different plasma procedures: for the first one the capacitively coupled power generator is solely used, and for the second one there is an additional inductively coupled power generator to increase the plasma density without simultaneously increasing the DC bias. Afterwards, an about 30 nm thick $Al_2O_3$ layer is deposited on the structured surfaces in an atomic layer deposition process to passivate the samples. Using scanning electron microscopy, reflection measurements and quasi steady state photoconductivity measurements to determine the effective minority charge carrier lifetime, the results are analyzed and differences and advantages are discussed.
Keywords: Plasma texturing, Reflectance, c-Si, Absorption, Lifetime

## 1 INTRODUCTION

The standard industrial texturing method for increasing the light absorption in crystalline silicon is a wet chemical etch process. Generally, pyramidal-shaped or similar structures are created. To reach much higher aspect ratios and thus to gain more light absorption, the so-called black silicon method is a promising process [1]. Further advantages of this dry, maskless plasma etch process are less silicon waste, no usage of fluid chemicals, better controllable etch treatment and the possibility to texture multicrystalline silicon with the same process. However, a strong increase of the effective surface area occurs; additional damage can be created during the plasma etch process because of ion bombardment which leads to an enhanced number of defects and to higher surface recombination [2,3,4]. This surface degradation makes an effective passivation step after the etching inevitable.

In this work, $SF_6$ and $O_2$ are applied as etch gases. In the plasma, F* radicals are formed which react isotropically with silicon to volatile $SiF_4$. For anisotropic etching, O* radicals act together with silicon and fluorine as a mask and a side wall passivation layer $SiF_xO_y$. A potential (DC bias) can be built between plasma and sample resulting in an acceleration of positive ions on the surface. So, there is an additional physical etching component. Due to this so called reactive ion etching (RIE) effect a preferred etch direction rectangle to the silicon surface is amplified. All in all, there must be an adequate balance between etching and passivation to produce structures of a high aspect ratio.

Within the last years, black silicon methods for PV applications were presented which use different plasma generation modes. As example, in [5,6,7,8,9], the RIE effect is utilized for etching deep structures by igniting the plasma capacitively with a plate electrode or similar setups. However, it is also demonstrated in [5,10] that with higher plasma power (and thus higher DC bias) as well as with longer etch time, the effective lifetime of charge carriers in the samples decreases strongly due to surface degradation.

In contrast to this ignition mode, in [11,12], the plasma is created with a microwave or inductively coupled generator, respectively. The advantage of both modes is the decoupling of the ion density in the plasma and the ion energy (DC bias). So, an increasing of the plasma power does not result in a higher DC bias.

Furthermore, up to now, no plasma process at temperatures above 0 °C exist, which reaches similar good reflection values and remains qualified for PV applications, as etch processes at temperatures below 0 °C; for example in [13], 91 % of the absorption of the Yablonovitch limit in the wavelength range from 300 nm to 1150 nm and effective lifetimes of 1 ms (passivated with an $Al_2O_3$ layer by thermal atomic layer deposition (ALD)) could be reached with black silicon wafers etched at -30 °C.

So in this work, two plasma processes with etch temperatures above 0 °C are presented:

- capacitively coupled plasma (CCP) at 5 °C
- inductively and capacitively coupled plasma (ICP+CCP) at 5 °C and 20 °C

The wafers are passivated analog to [12] with an about 30 nm thick $Al_2O_3$ layer deposited by thermal ALD.

Differences in optics, microstructure and effective lifetime between both processes are compared and discussed.

## 2 EXPERIMENTAL

To create textured silicon surfaces, an etch chamber of Oxford Instruments (Plasmalab System 100 ICP 65) is used. It includes a capacitively coupled power (CCP) generator as well as an inductively coupled power (ICP) generator at a 13.56 MHz radio frequency of a maximum power of 300 W and 600 W, respectively. The wafer is mechanically clamped on the lower electrode which can be cooled and heated. For an improved thermal contact between sample and electrode, Helium is supplied to the sample backside. The DC bias between the lower electrode and the wall chamber is measured in situ.

Monocrystalline, polished, p-doped FZ wafers with following properties are uses as material: resistivity 2 Ωcm, orientation <100>, thickness 250 µm.

The spectrally resolved reflection was measured with an integrating sphere to consider the diffuse and direct

reflection. Furthermore, the etch rate was estimated by weighing the samples before and after the etching and scanning electron microscopy (SEM) pictures of the etched wafers are recorded to observe the microstructure.

To investigate the influence of the surface recombination on the effective minority carrier lifetime, the wafers are etched on both sides. Afterward, they are cleaned with the standard RCA method; followed by the $Al_2O_3$ layer deposition by thermal ALD at 180 °C. To activate the $Al_2O_3$, the samples have to be annealed at 385 °C for 30 min. As example in **figure 1**, a SEM picture of a focused ion beam (FIB) cut shows a profile of an etched and passivated silicon wafer. The conformal passivation layer with a thickness of about 30 nm can clearly be identified.

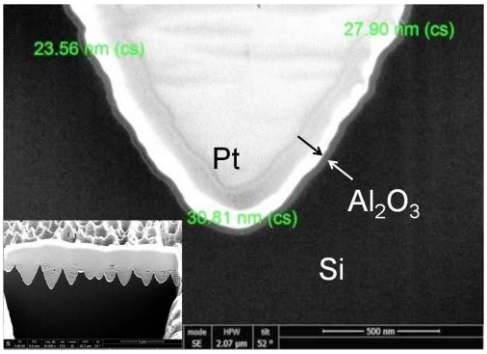


**Figure 1:** SEM picture of a FIB cut of a 15 min etched silicon sample at 5 °C (ICP+CCP) after passivation. The inset shows a lower magnification of this part. $Al_2O_3$ is the thin, dark grey layer between silicon (black) and platinum (white) which is needed for the FIB preparation.

The effective minority carrier lifetimes are measured after this passivation step using the quasi steady-state photoconductivity (QSSPC) method.

## 3 RESULTS

In this section, the optoelectrical properties of monocrystalline silicon wafers textured with both etch modes (CCP and ICP+CCP) are compared to each other. For this purpose, reflection spectra, SEM pictures and lifetime measurements are shown and discussed. It is started with the discussion of the experiments at 5 °C etch temperature. The etch process at ambient temperature is presented at the end.

To characterize the temporal trend during the texturing processes, the etch processes were stopped at different times. In **table I**, the varied etch times as well as the measured DC bias and etch rates are demonstrated for the CCP and ICP+CCP processes. The advantage of the ICP+CCP process is a higher etch rate. So, the wafer surface appears dark already after 7 min etching. To create comparable reflection results for the CCP process, the samples have to be etched more than 15 min. Furthermore, it is mentioned that the mean etch rate of the ICP+CCP process decreases with higher etch time from 2.0 µm/min at 7 min to 1.2 µm/min at 15 min; probably due to an increasing masking of the surfaces during the etching. The etch rate of the CCP process is comparatively very small (< 1 µm/min), which makes a more precise measurement difficult.

The DC bias of the ICP+CCP process is about the half of the DC bias values of the CCP process. So, the RIE effect should rather play a role for the CCP process, which should result in structures with higher aspect ratios, but also more surface damage.

**Table I:** Varied etch times, etch rate and DC bias during the CCP and ICP+CCP processes at 5 °C.

| | CCP | ICP+CCP |
|---|---|---|
| DC bias | ≈ 100 V | ≤ 50 V |
| etch rate | < 1.0 µm/min | 1.2 - 2.0 µm/min |
| etch time | 15, 25, 35, 45 min | 7, 10, 15 min |

### 3.1 Optics

In **figure 2**, the reflection spectra of the samples from both etch processes at 5 °C are shown. For ensuring better clearness, just one process per etch mode is presented: for the CCP process (blue lines) the etch time of 35 min is chosen, for the ICP+CCP process (red lines) 10 min. In contrast to the smooth unetched reference (black line), a strong antireflection is achieved for both processes (solid lines). With deposited passivation layer (dashed lines), the reflection of the wafer is additionally slightly reduced. For the CCP process, extremely low reflection values smaller than 1 % in the wavelength range till 1000 nm are reached; the samples etched with the ICP+CCP process reach at least about 2 % between 400 nm and 1000 nm. As comparison, the dotted line illustrates a reflection spectrum of an alkaline etched silicon wafer. It does not even reach values under 10 %. This difference between the wet chemical and the plasma texturing processes in the reflection proves the optical advantage of the dry plasma method for silicon with respect to PV applications.

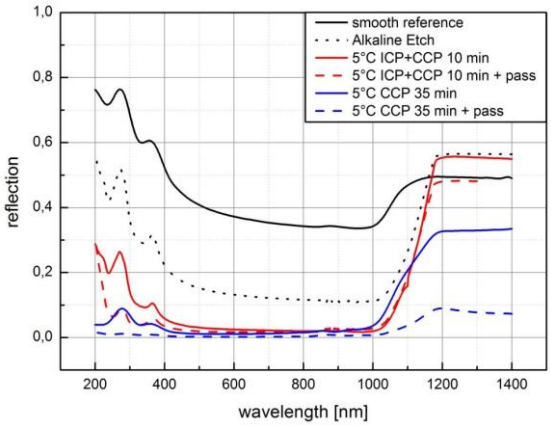


**Figure 2:** Reflection spectra: black line – untreated smooth reference; dotted line – alkaline etched wafer; solid lines – before passivation, dashed lines – after passivation; blue lines – CCP process 35 min etched; red lines – ICP+CCP process 10 min etched.

### 3.2 Microstructure

To investigate the structural shape of the etched wafers, SEM pictures are presented in **figure 3**. For both etch processes, the top and side view is recorded. Please note the different magnifications in the pictures. For

orientation, the mark at the top left corner of every picture is equal to 1 µm.

Regarding the CCP process (left pictures, 45 min etched), needle like structures are created during the etching. Similar shapes are formed when decreasing the etch length. The averaged distance of the structures is in the range of 100 nm to 170 nm and the aspect ratios are between 5:1 after 15 min etching and 3:1 after 45 min.

Performing the etching with the ICP+CCP process (right pictures), holes are etched into the surface in contrast to the needles or cones of the CCP process. The averaged distance of the structures is one order of magnitude higher (about 1 µm) and the aspect ratio is rather small (2:1). This values are rather independent of the etch time.

Nevertheless, both textures – though very different – cause a significant reflection decline.

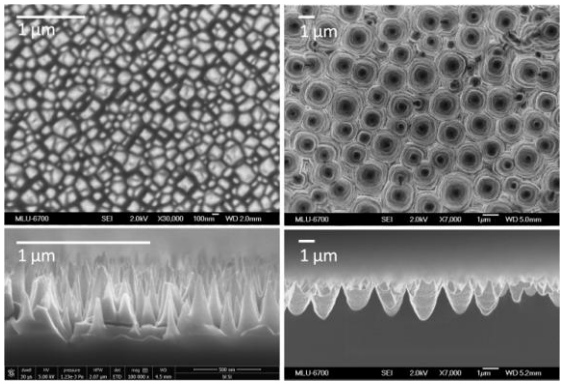


**Figure 3:** SEM picture from vertical view (above) and in profile (below): CCP process after 45 min etching (left) and ICP+CCP process after 10 min etching (right).

3.3 Effective minority carrier lifetime

After depositing the passivation layer $Al_2O_3$ by a thermal ALD process, the effective minority carrier lifetime is measured by QSSPC. The results of the QSSPC measurement of all etched samples are shown in **figure 4**: To compare the lifetimes of the etched wafer, a smooth reference wafer is also included (dark crosses): 4.5 ms are reached at a minority carrier density of $10^{15}$ $cm^{-3}$.

As first observation for both etch processes, the lifetime decreases with increasing etch length due to a longer exposure to the plasma which was also observed in [5].

In contrast to the good reflection properties, the lifetimes of the CCP process show a strong decline to values of about 10 µs. As explanation for this decrease, the high DC bias of about 100 V should be mentioned. It seems like the accelerated ions affect the surface very strongly resulting in a high degradation.

For the ICP+CCP process, very high lifetimes between 3.6 ms (7 min etched) and 1.7 ms (15 min etched) can be achieved. With regard to the CCP process, there is a great improvement, which could – at least partially- be explained by the lower DC bias of about 53 V.

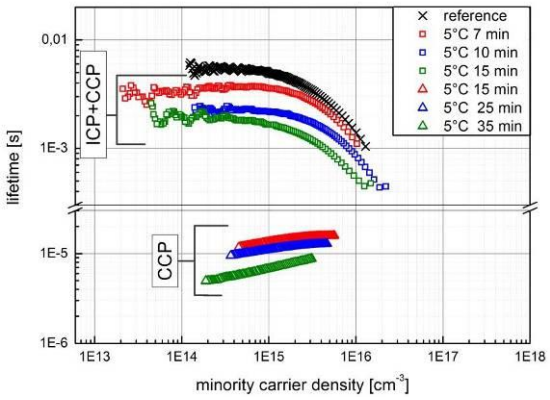


**Figure 4:** The effective minority carrier lifetime against the minority carrier density after passivation is plotted for a smooth reference: black crosses, the ICP+CCP process: squares (7 min – red, 10 min – blue, 15 min – green) and the CCP process: triangles (15 min – red, 25 min – blue, 35 min – green).

3.4 Reflection versus lifetime

The measured values of every etch process is tabularized in **table II**, including the data of a 20 °C ICP+CCP process. In contrast to the experiment at 5 °C, the DC bias is lower, but reflection and lifetime are worse. So, the surface seems to be more damaged during the etch process at higher temperatures although the DC bias is lower. Furthermore, the etched structures look similar to the ICP+CCP process at 5 °C, but the aspect ratios are smaller. This should be the reason for the higher reflection values.

**Table II**: Table of the averaged reflection (300 nm - 1000 nm), lifetime (at $10^{15}$ $cm^{-3}$) and DC bias of all processes.

| | CCP (5 °C) | | | | ICP+CCP (5 °C) | | | ICP+CCP (20 °C) | |
|---|---|---|---|---|---|---|---|---|---|
| etch time (min) | 15 | 25 | 35 | 45 | 7 | 10 | 15 | 10 | 15 |
| reflection (%) | 1.9 | 0.7 | 0.4 | 0.4 | 3.1 | 2.4 | 2.1 | 4.8 | 3.8 |
| lifetime (µs) | 13 | 11 | 7 | - | 3623 | 2187 | 1674 | 1761 | 1489 |
| DC bias (V) | 98 | 95 | 95 | 92 | 53 | 126 | 52 | 34 | 33 |

To compare both parameters, the effective lifetime versus reflection values are demonstrated in **figure 5**. Here, one can clearly see that with increasing etch time, the reflection and lifetime is decreased. Furthermore, the distinction between the two etch processes is shown: samples prepared with the CCP process reach very low reflection of 0.5 %, but also small lifetimes of about 10 µs. Whereas, higher reflection (2.1 %), but extremely high lifetimes > 1 ms are created with the ICP+CCP process.

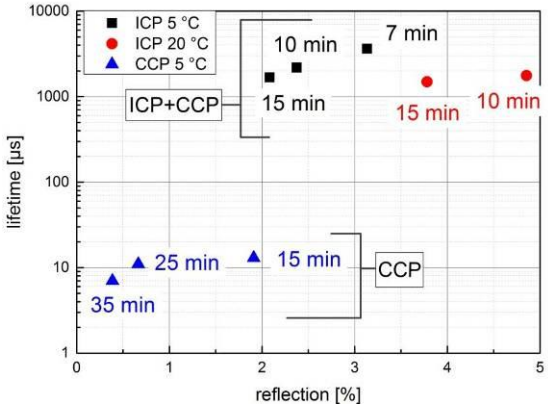


**Figure 5**: Effective lifetime plotted against the averaged reflection for the CCP process etched at 5 °C (blue triangles) and the ICP+CCP process etched at 5 °C (black squares) and 20 °C (red cycles). The assigned times in minutes indicate the etch lengths.

## 4 CONCLUSION

In this work, the optics, microstructure and effective lifetime of two different maskless plasma processes for texturing monocrystalline silicon at temperatures above 0 °C are compared. The attention was focused on the ignition mode: capacitive (CCP) or inductive and capacitive (ICP+CCP) plasma generation. It applies for both processes that with increasing etch time the reflection is reduced, but also the lifetime.

With the CCP process, very small reflection values < 1 % can be achieved due to needle like structures with high aspect ratios. But only wafers etched with the ICP+CCP process reach lifetimes above 1 ms. So, all in all, black silicon for PV applications etched at temperatures above 0 °C is possible for the ICP+CCP process.

## 5 ACKNOWLEDGEMENT

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